UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/537,786	03/29/2000	Masatsugu Fujii	FUJX17,182	7367

			EXAMINER
26304	7590	01/30/2004	CHOW, CHARLES CHIANG

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ART UNIT	PAPER NUMBER
2685	

DATE MAILED: 01/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>06 November 2003</u>.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) <u>1-16</u> is/are pending in the application.

  4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) <u>1-16</u> is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

  Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

  Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

  a)☐ All b)☐ Some * c)☐ None of:

    1.☐ Certified copies of the priority documents have been received.

    2.☐ Certified copies of the priority documents have been received in Application No. _____.

    3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

  * See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

  a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .

4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: .

Office Action for
Applicant's Amendment
Received on 11/06/2003

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1, 2, 8, 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Titchener

    (US 4,670,890) in view of Kawazoe et al. (US 5,327,441).

    Regarding **claim 1**, Titchener teaches a coding assisting equipment (as the apparatus and

    method for encoding and decoding codes, abstract, figure in cover page, Fig. 1-10, for

    transmitting variable length coded string of data, abstract, and for enabling easy

    synchronization for decoding, col. 1, lines 7-14; summary of invention, col. 1, line 56 to col.

    3, line 31).

    Titchener teaches the operating-object holding means for sequentially holding each word

    respectively consisting of plural bits (as the (c) buffer means for buffering each selected input

    code sequentially in turn , col. 45, lines 12-13).

    Titchener teaches the constant word length (as the (a) an input buffer means for receiving

    each fixed length symbol to be converted to variable length symbols wherein the length of

    the fixed length code is m+1 (col. 46, lines 40-43).

    Titchener teaches the argument holding means for holding an argument applied to an

operation that is performed on a word that is subsequently held by operating–object holding means (as the augment code buffer 33 applied to prefixing coding operating, figure in cover page; the augment code buffer 22 holds the incoming augment code from the input code 29 set, as the claimed operating-object holding means, as shown in figure in cover page; the original character set C^0 is augmented 9 times until C^q is exhansted, abstract, col. 41, lines 11-67).

Titchener teaches the that is included in said word being held by operating-object holding means and/or the result performed in advanced being held by operation-object holding means (the input code set 29 is holding the augment code result performed in advanced before receiving the next output code set on input 36 to be operated with the input 26, base set, figure in cover page, col. 41, lines 28-38).

Titchener teaches the holding an argument for an operation that is performed on a word that is subsequently held by the operating-object holding means, and the argument being include in said word being held by said operating object holding means and/or results of an operation performed in advance on the word being held by said operation-object means, the augmented code for generating variable length code by holding input code in the 29 (the inputting source code into memory means col. 47, lines 20-22, abstract, Fig. 6b, Fig. 8) for the objection for logic operation, and the subsequent augment codes, $C^1 \ldots C^{q-1}$, coming from output code set 35 (Fig. 6b) to applying code augmentation at 29 with input base set 28 (Fig. 6b) for the argument being applied to the subsequent operation. Titchener teaches the word is added a bit fed sequentially by monitoring and augmenting each bit to word C^0 to C^q (col. 40, lines 25-35), and augmented binary codes (col. 9, line 55 to col. 10, line 25).

Titchener does not clearly teach the logical operation on a combination of logic values.

Regarding the logic operation on to be performed on a combination of logic values and

the convolutional encoding, Kawazoe et al. ("Kawazoe") teaches the simple convolutional

encoder and decoder of arbitrary length with arbitrary coding rate (col. 3, 40-43, col. 3, lines

40-68; col. 13, lines 20-53). Kawazoe teaches the logic operation to be performed on

combination logic value for the convolutional encoder (as shown in Fig. 4-5, col. 4. line 46 to

col. 7, line 59). Kawazoe teaches the convolutional decoder with logic operation and

combination logic value (as shown in Fig. 12, col. 4, lines 33-36). Kawazoe teaches an

efficient convolutional encoder/decoder, such that the encoder/decoder can be simpler (col. 3,

lines 26-43). Therefore, it would have been obvious to one of ordinary

skill in the art at the time of invention to modify and include Titchener and to include

Kawazoe's logic operation and combination logic for the convolutional encoder/decoder,

such that the digital processing could be efficient on encoding and decoding.

Regarding **claim 2**, Titchener teaches a decoding assisting equipment (as the apparatus and

method for encoding and decoding codes, abstract, figure in cover page, Fig. 1-10, for

transmitting variable length coded string of data, abstract, and for enabling easy

synchronization for decoding, col. 1, lines 7-14; summary of invention, col. 1, line 56 to col.

3, line 31). Titchener teaches the operating-object holding means for sequentially holding

each word respectively consisting of plural bits (as the (c) buffer means for buffering each

selected input code sequentially in turn , col. 45, lines 12-13). Titchener teaches the constant

word length (as the (a) an input buffer means for receiving each fixed length symbol to be

converted to variable length symbols wherein the length of the fixed length code is m+1 (col.

46, lines 40-43). Titchener teaches the argument holding means for holding an argument

applied to an operation that is performed on a word that is subsequently held by operating–

object holding means (as the augment code buffer 33 applied to prefixing coding operating,

figure in cover page; the augment code buffer 22 holds the incoming augment code from the

input code 29 set, as the claimed operating-object holding means, as shown in figure in cover

page; the original character set C^0 is augmented 9 times until C^q is exhansted, abstract, col.

41, lines 11-67). Titchener teaches the that is included in said word being held by operating-

object holding means and/or the result performed in advanced being held by operation-object

holding means (the input code set 29 is holding the augment code result performed in

advanced before receiving the next output code set on input 36 to be operated with the input

26, base set, figure in cover page, col. 41, lines 28-38).

Titchener teaches the holding an argument for an operation that is performed on a word that

is subsequently held by the operating-object holding means, and the argument being include

in said word being held by said operating object holding means and/or results of an operation

performed in advance on the word being held by said operation-object means, the augmented

code for generating variable length code by holding input code in the 29 (the inputting source

code into memory means col. 47, lines 20-22, abstract, Fig. 6b, Fig. 8) for the objection for

logic operation, and the subsequent augment codes, $C^1...C^{q-1}$, coming from output code set

35 (Fig. 6b) to applying code augmentation at 29 with input base set 28 (Fig. 6b) for the

argument being applied to the subsequent operation. Titchener teaches the word is added a

bit fed sequentially by monitoring and augmenting each bit to word C^0 to C^q (col. 40, lines

25-35), and augmented binary codes (col. 9, line 55 to col. 10, line 25).

Titchener does not clearly teach the logical operation on a combination of logic values.
Regarding the logic operation on to be performed on a combination of logic values and
the convolutional encoding, Kawazoe et al. ("Kawazoe") teaches the simple convolutional
encoder and decoder of arbitrary length with arbitrary coding rate (col. 3, 40-43, col. 3, lines
40-68; col. 13, lines 20-53). Kawazoe teaches the logic operation to be performed on
combination logic value for the convolutional encoder (as shown in Fig. 4-5, col. 4. line 46 to
col. 7, line 59). Kawazoe teaches the convolutional decoder with logic operation and
combination logic value (as shown in Fig. 12, col. 4, lines 33-36). Kawazoe teaches an
efficient convolutional encoder/decoder, such that the encoder/decoder can be simpler (col. 3,
lines 26-43). Therefore, it would have been obvious to one of ordinary
skill in the art at the time of invention to modify and include Titchener and to include
Kawazoe's logic operation and combination logic for the convolutional encoder/decoder,
such that the digital processing could be efficient on encoding and decoding.

Regarding **claim 8**, Titchener has taught above the sequential operation for adjusting
augmented code for generating variable augmented codes.

Regarding **claim 13**, Titchener teaches the decoding assisting equipment above, the word
length adjusting means for converting the result to target amount of codes; the operation
means into a sequence of constant fixed length for sequentially supplying to a subsequent
predetermined operation means.

2. Claims 3, 4, 6, 7, 9, 11, 12, 14 rejected under 35 U.S.C. 103(a) as being unpatentable over

Titchener in view of Kawazoe, as applied to claims 1, 2 above, and further in view of Lan et

al. (US 5,787,099).

Titchener and Kawazoe do not clearly teach the highest term in the polynomial is smaller

than or equal to said word length.

Regarding **claim 3**, Lan teaches the system and method for encoding and decoding data using

numerical computation in Galois fields (title). The integrated circuits and combinational logic

(figure in cover page, Fig. 1-20b) contains the encoder/decoder 101 and holding register 105,

for using multiplies to detect/correct errors in certain position (abstract). Lan considers the

highest term in a polynomial is smaller than said word length, as to be the: for each code

word (n symbol positions, k data positions), the check symbols are the coefficients of the

remainder polynomial generated by dividing the polynomial of (n-1) order by the polynomial

of order (n-k), such that the check symbols from the remainder could fit into (n-k-1) positions

of the n symbols coded word (in col. 1, lines 44-63), such that the check symbols would fill

up the remaining positions in each code with n symbol positions and k data positions. Lan

teaches the technique for coding the symbols with check symbol without exceeding the

maximum available n symbol positions, such that, at least the encoder/decoder could be

upgraded and supplying the check symbols for error correction without exceeding maximum

available n symbol positions. Therefore, it would have been obvious to one of ordinary skill

in the art at the time of invention to modify Titchener, and to include Lan's technique for

coding the symbols with check symbol without exceeding the maximum available n symbol

positions, such that, at least the encoder/decoder could be upgraded and supplying the check symbols for error correction without exceeding maximum available n symbol positions. Regarding the operating-object holding means fed with pieces of transmission information divided into constant fixed length symbols, referring to examiner's comment in claim 1 above.

Regarding **claim 4**, referring to examiner's comment in claims 1-3 above for the decoding assistant equipment said operating-object holding means receives fixed length symbols; and the for each code word (n symbol positions, k data positions), the check symbols are the coefficients of the remainder polynomial generated by dividing the polynomial of (n-1) order by the polynomial of order (n-k), such that the check symbols from the remainder could fit into (n-k-1) positions of the n symbols coded word (in col. 1, lines 44-63), such that the check symbols would fill up the remaining positions in each code with n symbol positions and k data positions. Regarding the operating-object. holding means fed with pieces of transmission information divided into constant fixed length symbols, referring to claim 1 above.

Regarding **claim 6**, Titchener has taught above the adding bit at the end of code word at each level of augment, and the prefixing processing for adding bit before the most significant bit, for generating augmented variable length code.

Regarding **claim 7**, Titchener teaches the invalid bit string, the block code contains some redundancy (col. 12, lines 55-61), the adding redundancy in other coding scheme for correct synchronization (col. 22, lines 44-57).

Regarding **claims 9, 11,** Titchener has taught above in claim 1 for the decoding assisting

equipment above, the word length adjusting means for converting the result to target amount

of codes; the operation means into a sequence of constant fixed length for sequentially

supplying to a subsequent predetermined operation means.

Regarding **claim 12,** Titchener has taught above in claim 1 for the decoding assisting

equipment above, the word length adjusting means for converting the result to target amount

of codes; the operation means into a sequence of constant fixed length for sequentially

supplying to a subsequent predetermined operation means.

Regarding **claim 14** Titchener teaches the decoding assisting equipment above, the word

length adjusting means for converting the result to target amount of codes; the operation

means into a sequence of constant fixed length for sequentially supplying to a subsequent

predetermined operation means.

3. Claims 5, 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Titchener in

    view of Kawazoe, as applied to claim 1 above, and further in view of Kindred et al. (US

    5,710,784).

    Titchener and Kawazoe do not clearly teach the tree codes and the constraint of shorter word

    length.

    Regarding **claim 5,** Kindred teaches the viterbi decoder for CDMA system (title, abstract,

    figure in cover page), comprising the rf interface receiver 24, the demodulator 26, the

    interleaver 32. The decoder, with input/output buffer, could simultaneously decoding at

multiple packet data rate, creating quality metric. The decoder could be reconfigured for different convolutional encoding algorithms (abstract, Fig. 5, col. 1, lines 21-25). Kindred considers the tree code has the length constraint k in col. 9, lines 35-47, for reducing the number of global sequences and selecting the best local path for generating the convolutional codes. Kindred considers the tree code with length constraint k such that the best path for generating the code from the tree structured codes. It is apparently obvious to include Kindred's technique for selecting the proper sequence and best path for generating the convolutional tree codes, to Titchener, such that the system could be upgraded for efficiently generating the tree code by utilizing Kindred's technique. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention, essentially if not obvious, to modify and include Kindred's technique for selecting the proper sequence and best path for generating the convolutional tree codes, to Titchener as modified above, such that the system could be upgraded for efficiently generating the tree code by utilizing Kindred's technique. Regarding the operating-obj. holding means fed with pieces of transmission information divided into constant fixed length symbols, referring to claim 1 above. Regarding **claim 10**, Titchener has taught above in claim 1 for the decoding assisting equipment above, the word length adjusting means for converting the result to target amount of codes; the operation means into a sequence of constant fixed length for sequentially supplying to a subsequent predetermined operation means.

6. Claim 15, 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Titchener in view of Kawazoe, and further in view of Astrachan (US 5,612,974).

Regarding **claim 15**, Titchener and Kawazoe has taught above all other claimed features,

except the radio transmitter, the radio receiver, the wireless interface, the encoder/decoder.

However, Astrachan teaches the single integrated circuit for performing multitude of

communication tasks (col. 1, lines 7-11) having radio transmitter and receiver for the

communication unit 10. The communication unit 10 contains the RF interface for

transmitting and receiving signals via antenna 14 for the wireless interface to the TDAM,

CDMA network, col. 4, lines 61-65). The communication 10 comprises rf interface 16,

demodulator 18, block decode 202 (Fig. 5). The communication device 10, comprises the

block encoder 228, the encoded stream 146, the modulator 34 (Fig. 6). Astrachan teaches the

communication unit 10 comprising the block encoder/decoder for rf communication with the

wireless, TDMA, CDMA networks, to Ttichener, such that the message or information could

be obviously transmitted and received via the rf communication channels. Therefore, it

would have been obvious to one of ordinary skill in the art at the time of invention,

essentially if not obvious, to modify and include Astrachan's communication unit 10

comprising the block encoder/decoder for rf communication with the wireless, TDMA,

CDMA networks, to Ttichener as modified above, such that the message or information

could be obviously transmitted and received via the rf communication channels.

Regarding **claim 16**, Titchener and Kawazoe has taught above all other claimed features,

except the radio transmitter, the radio receiver, the wireless interface, the encoder/decoder.

Astrachan has taught above the radio receiver; the wireless interface; the operating–object

holding means; the argument holding means; the operation means and the combination of said logic values.

Response to Argument

7. Applicant's arguments with respect to claims 1-16 have been considered but are moot in view of the new ground(s) of rejection.

Regarding applicant's argument for the no teachings for the object being subject for logic operation, the argument being applied to subsequent operation, the word is added a bit being fed sequentially (applicant's remark, page 2, last two line to page3, first two lines), Titchener-'890 teaches the augmented code for generating variable length code by holding input code in the 29 (the inputting source code into memory means col. 47, lines 20-22, abstract, Fig. 6b, Fig. 8) for the objection for logic operation, and the subsequent augment codes, $C^1...C^{q-1}$, coming from output code set 35 (Fig. 6b) to applying code augmentation at 29 with input base set 28 (Fig. 6b) for the argument being applied to the subsequent operation. Titchener teaches the word is added a bit fed sequentially by monitoring and augmenting each bit to word C^0 to C^q (col. 40, lines 25-35), and augmented binary codes (col. 9, line 55 to col. 10, line 25). In view of the above teachings from Titchener-890, pending claims are remaining in rejection manner. For the coding/decoding in communication technology, it is well-known that the coder/decoder can be operated at high speed without changing hardware for increasing efficiency, reliability, for improving processing delay, saving memory spacing and with less power consumption. Kawazoe teaches the polynomial for decoding, encoding, having constrain K for controlling the length of generating polynomial (abstract; col. 3, lines 47-68; col. 17, line 66 to col. 18, line 5). In view of above teachings, claims 1-16 are

remaining in the rejection manner.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner

should be directed to Charles Chow whose telephone number is (703)-306-5615.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor,

Edward Urban, can be reached at (703)-305-4385.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks
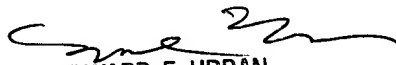
Washington, D.C. 20231

or faxed to: (703) 872-9306 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive,

Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding

should be directed to the Technology Center 2600 Customer Service Office whose telephone

number is (703) 306-0377.

Charles Chow $C.C.$,

January 6, 2004.

EDWARD F. URBAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600